

FIG. 1A

FIG. 1B

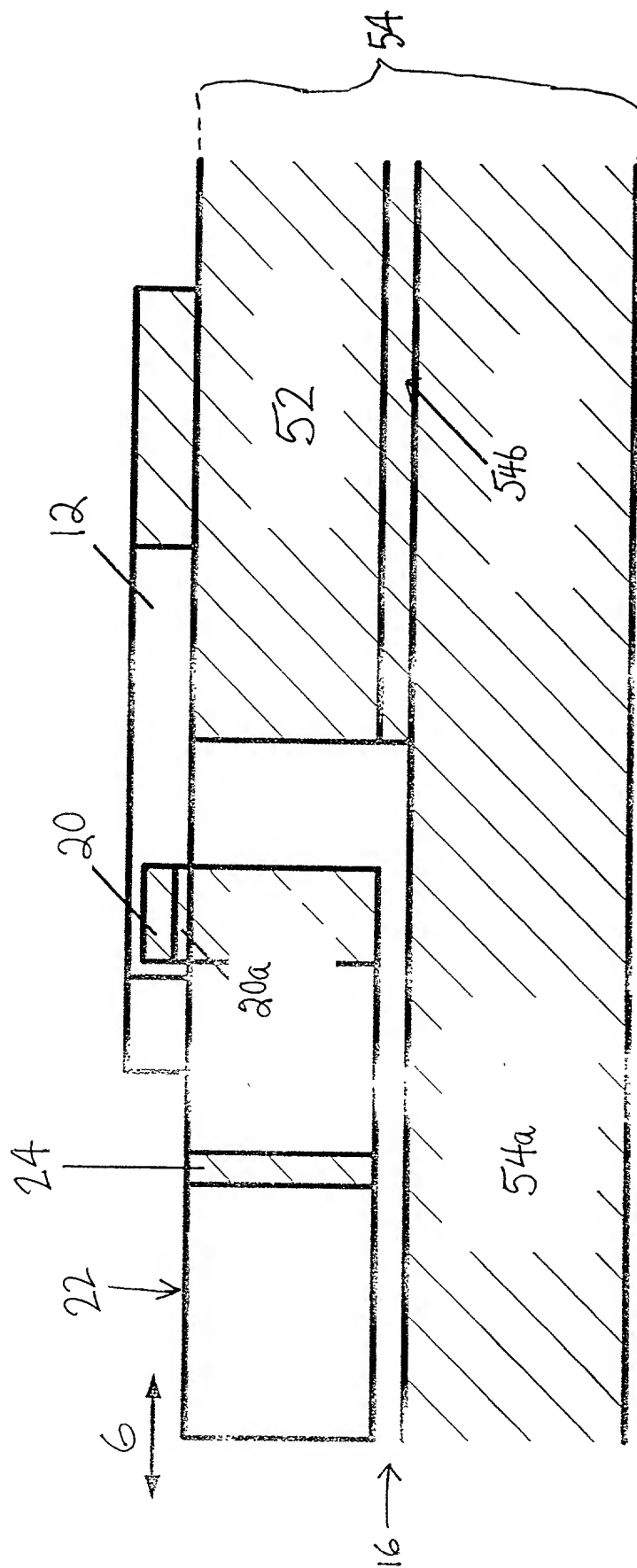


FIG. 1C

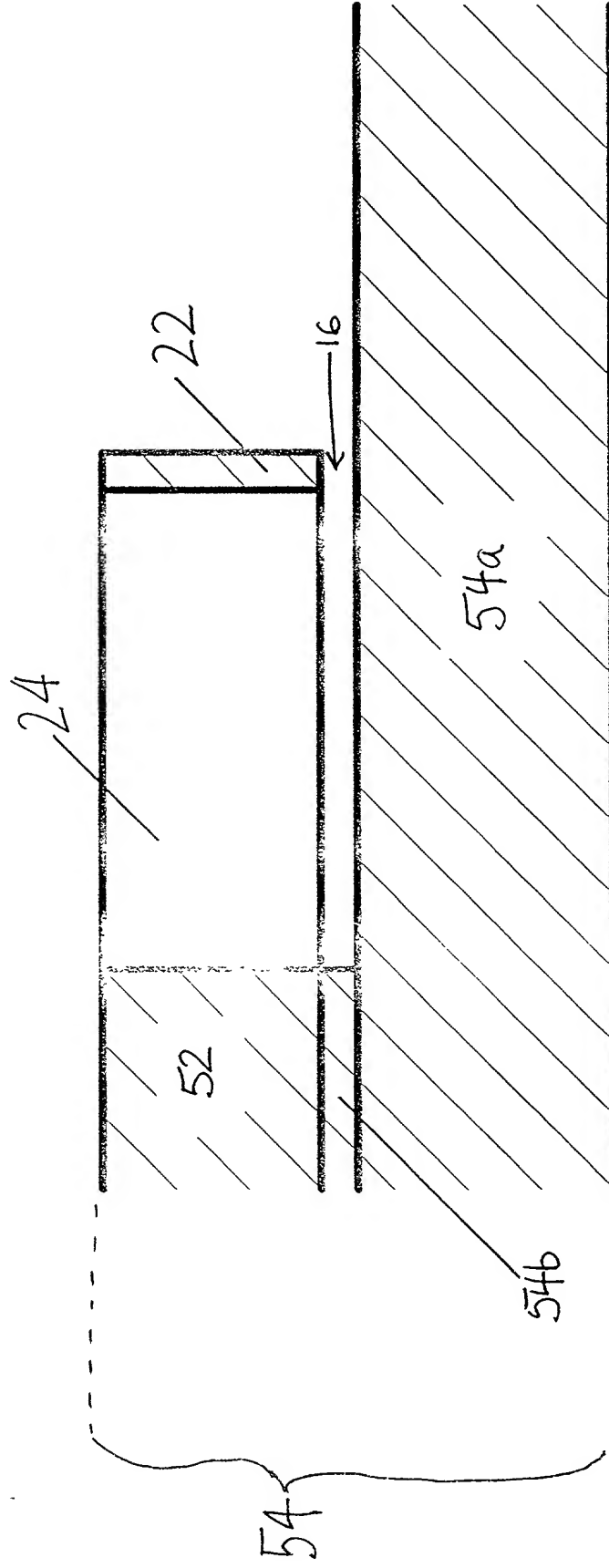
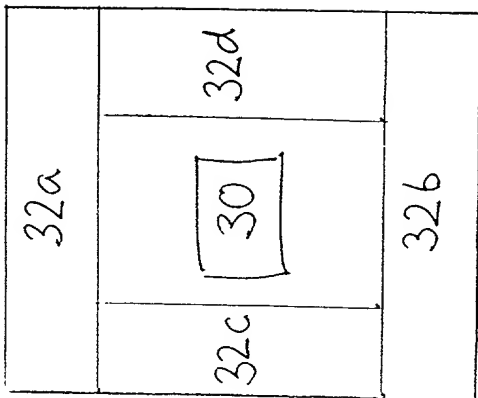


FIG. 2B



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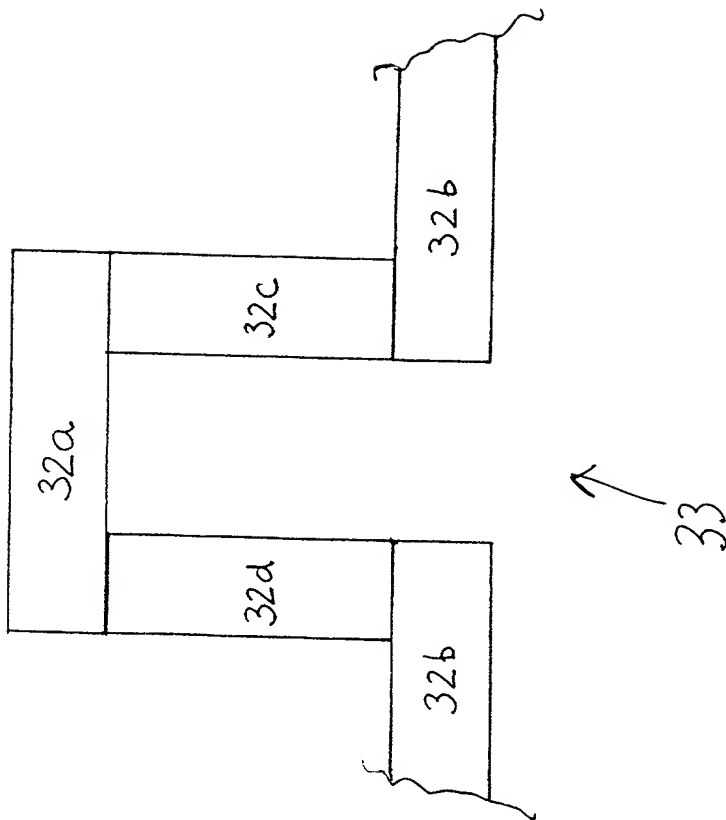


FIG. 20

FIG. 2D

10079985.022107

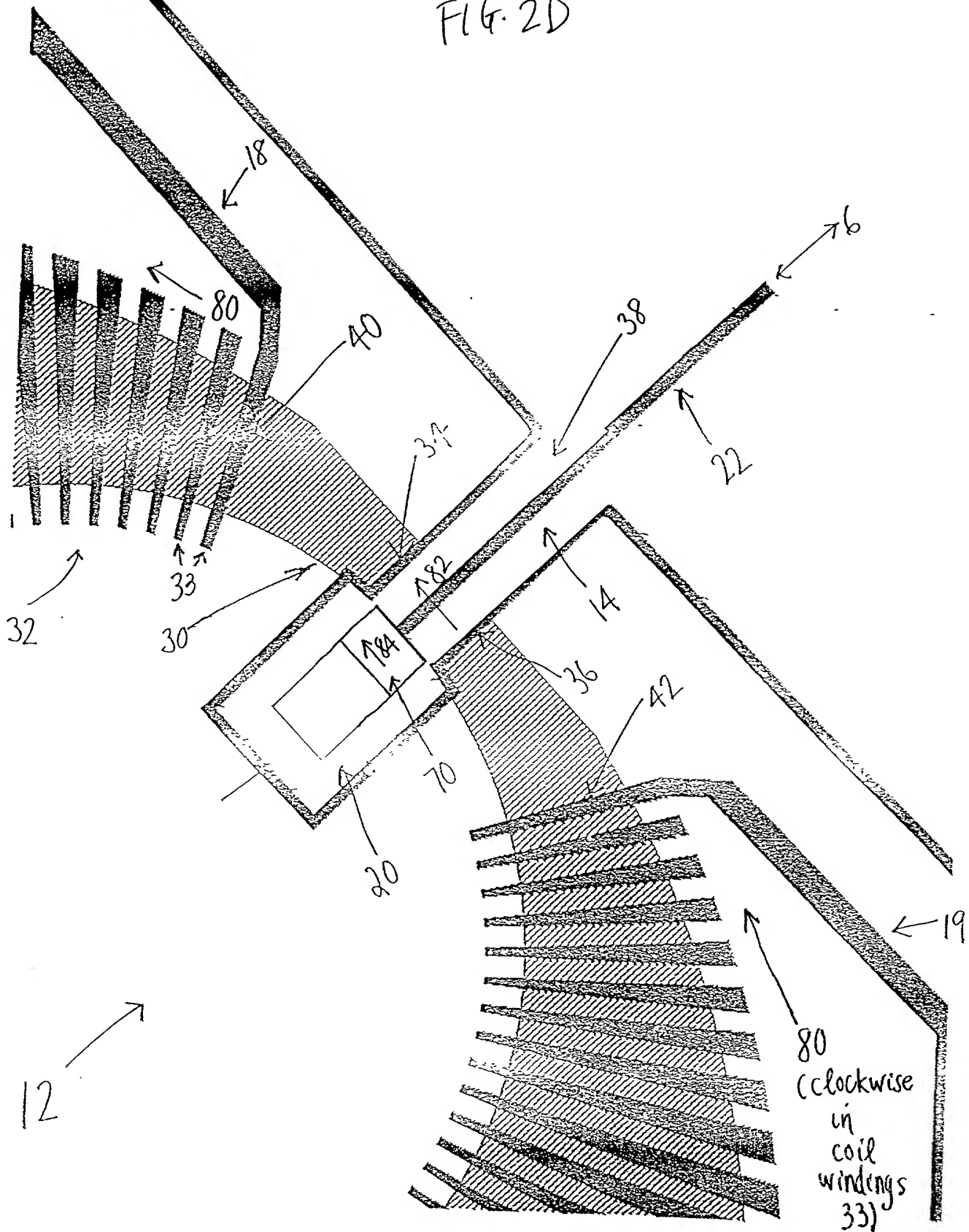
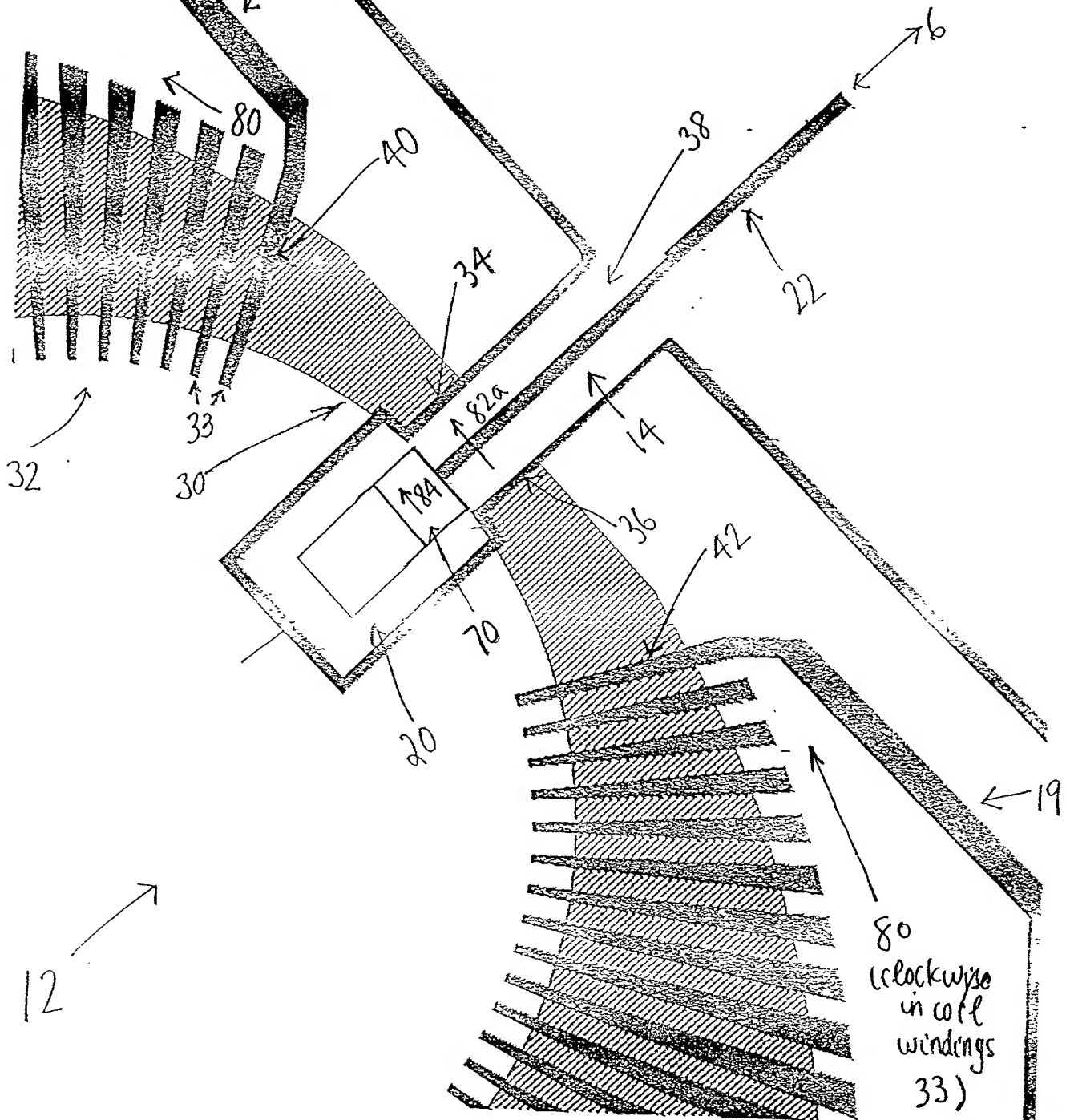
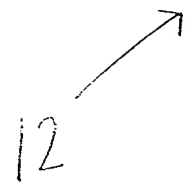


FIG. 3A



10079985-02102

[illegible]

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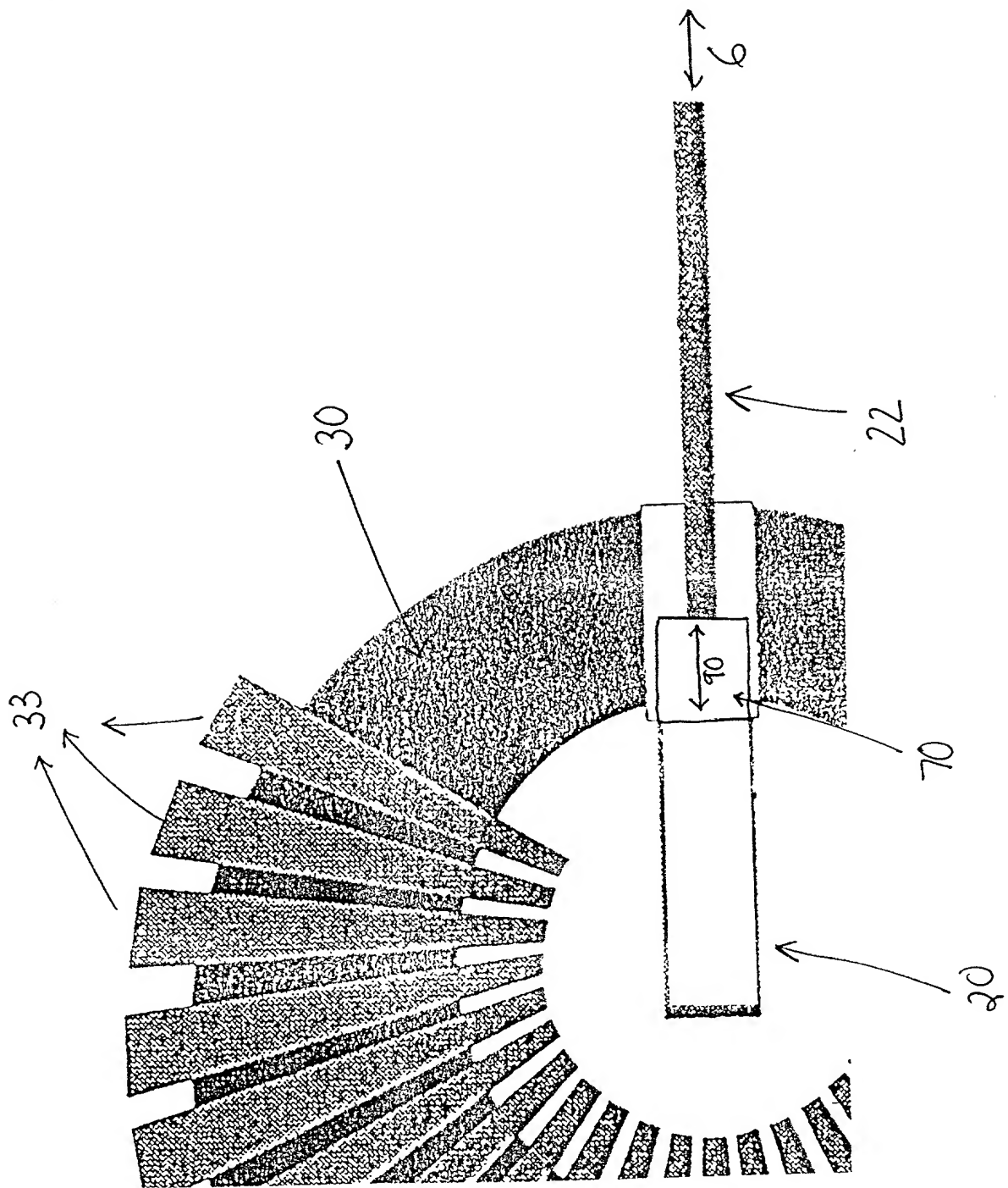


Fig. 4A

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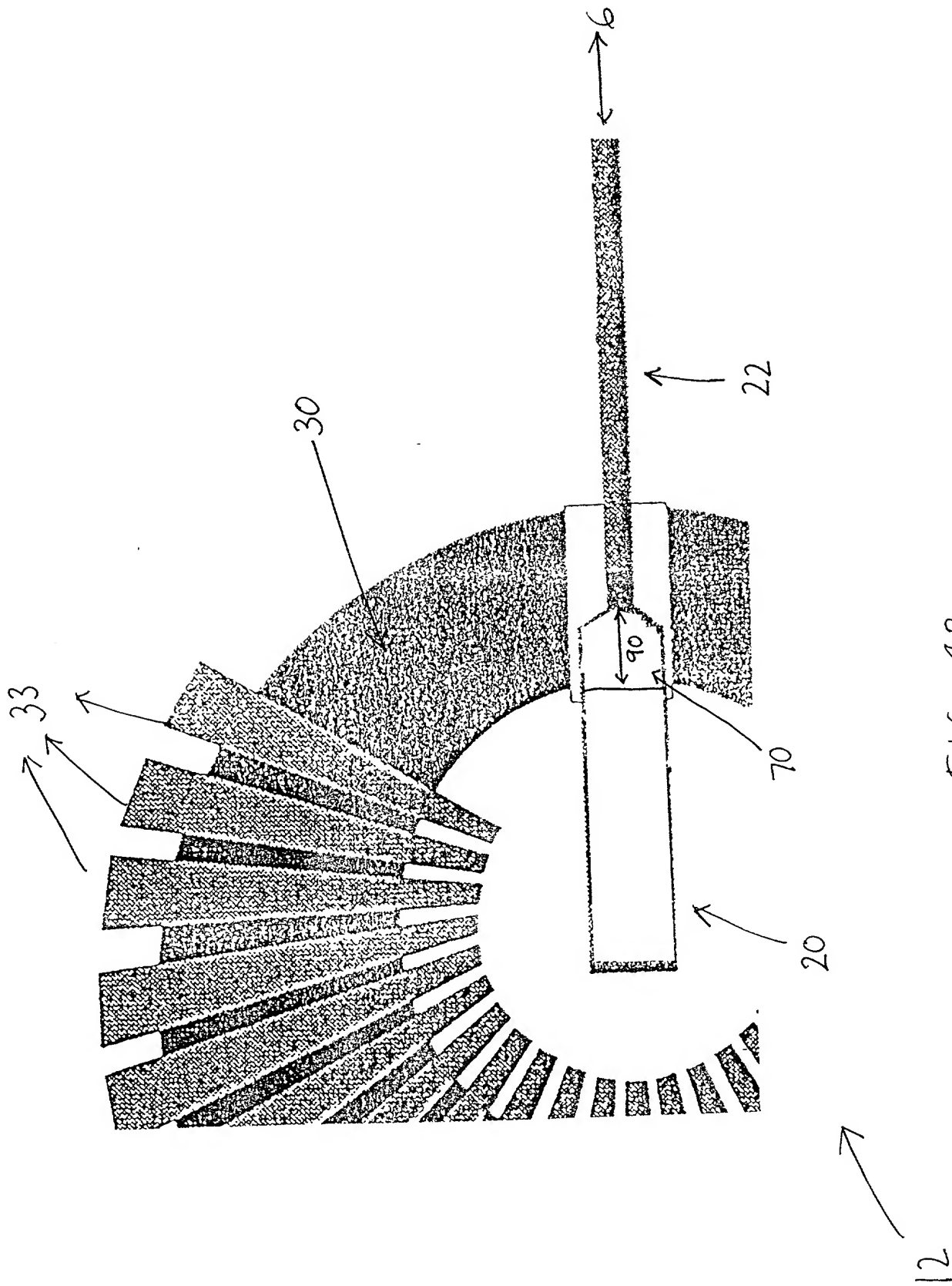
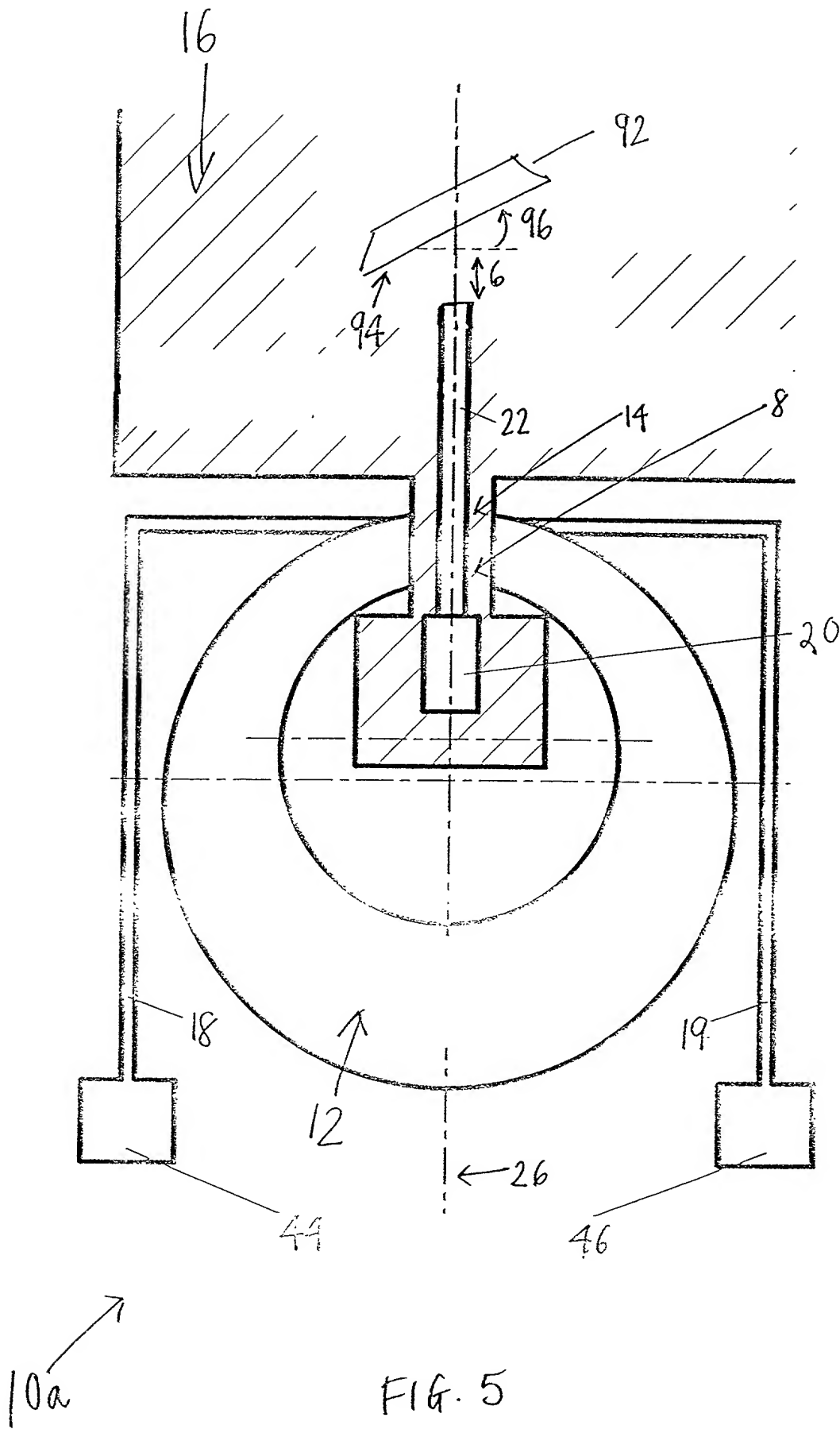
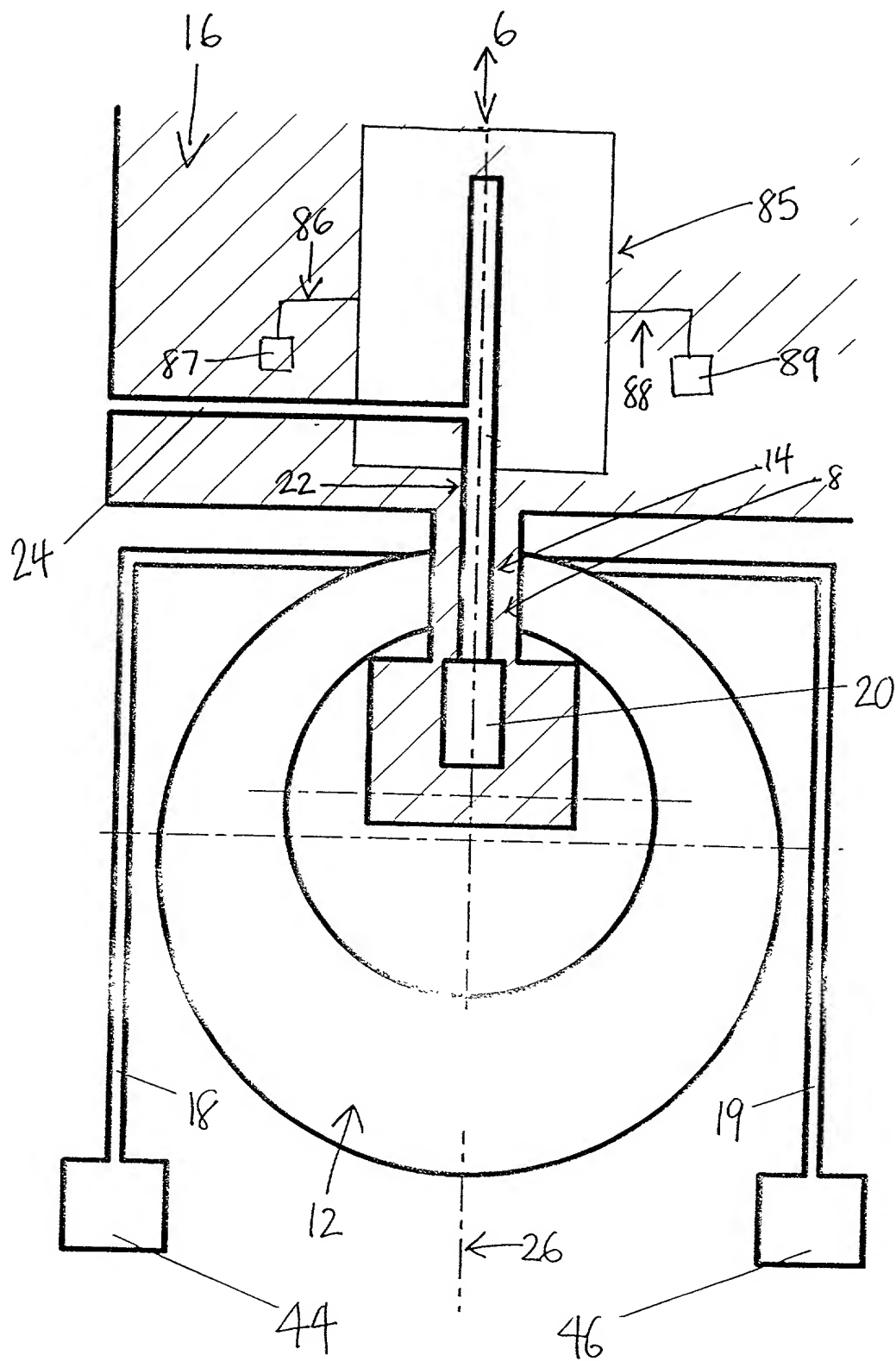


FIG. 4B

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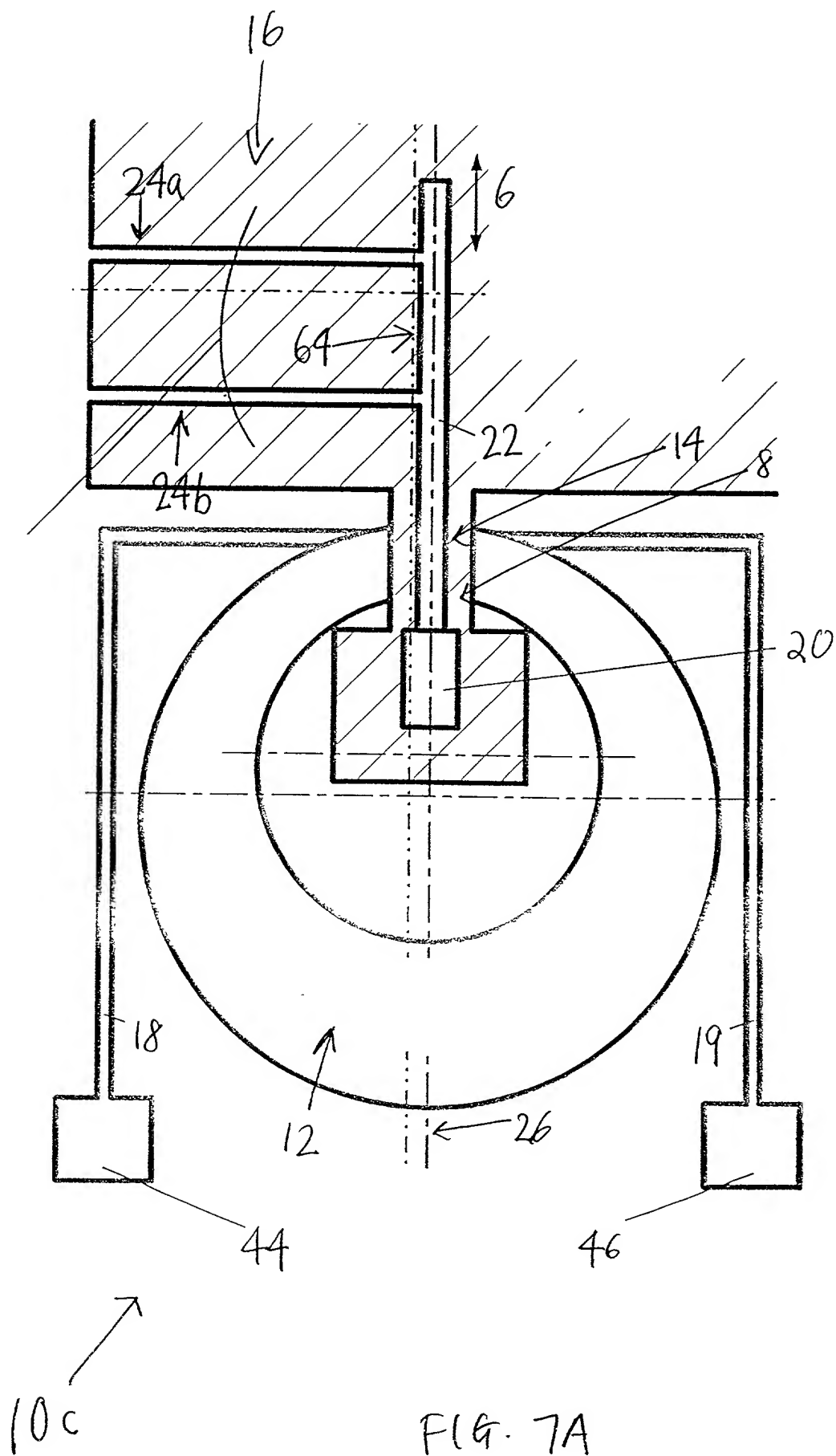





106

FIG. 6

10079985.022102



10d 

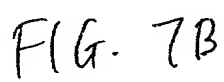
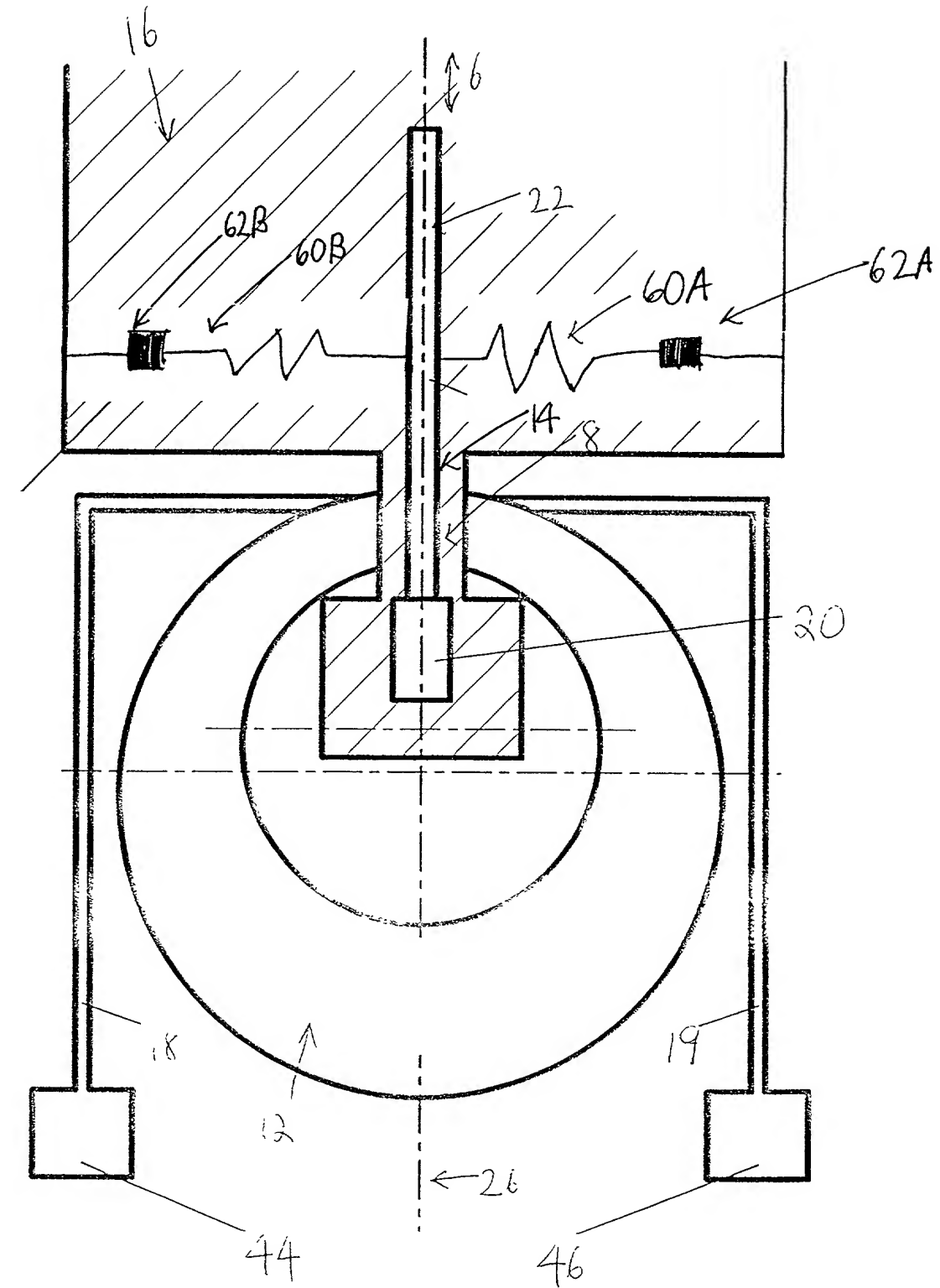


FIG. 8A

10079989, 022103



10f

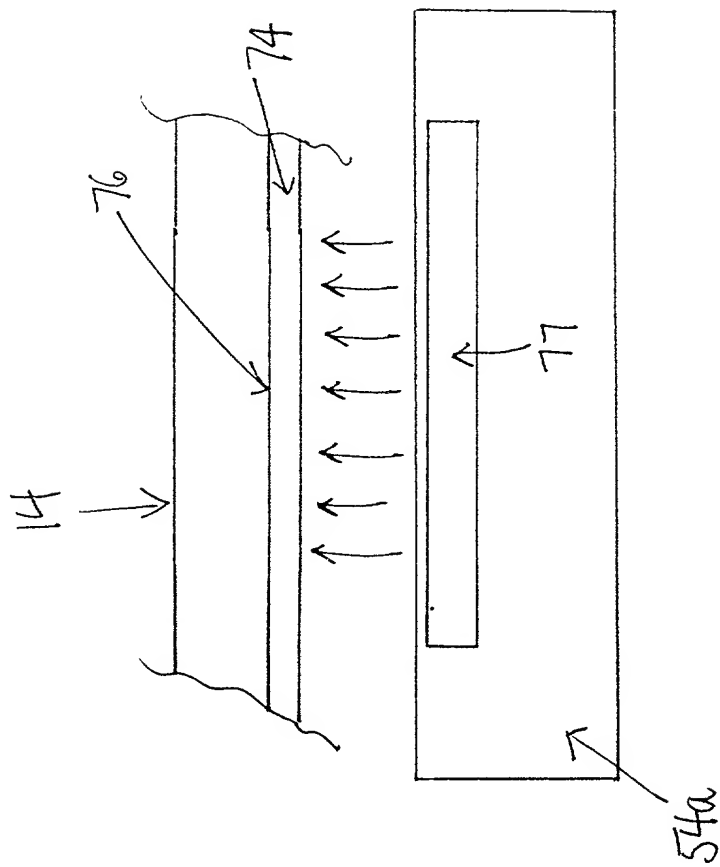


FIG. 9A

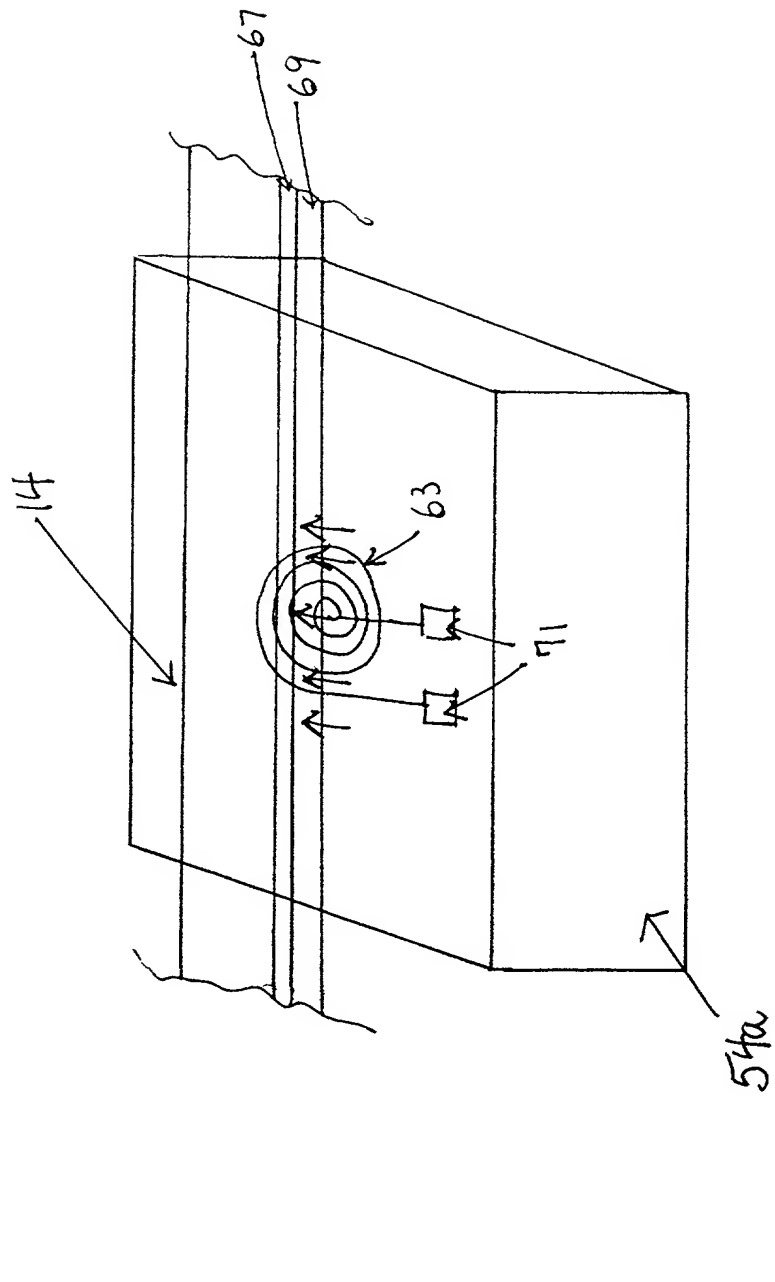


FIG. 9B

FIG. 10

10079965-000100

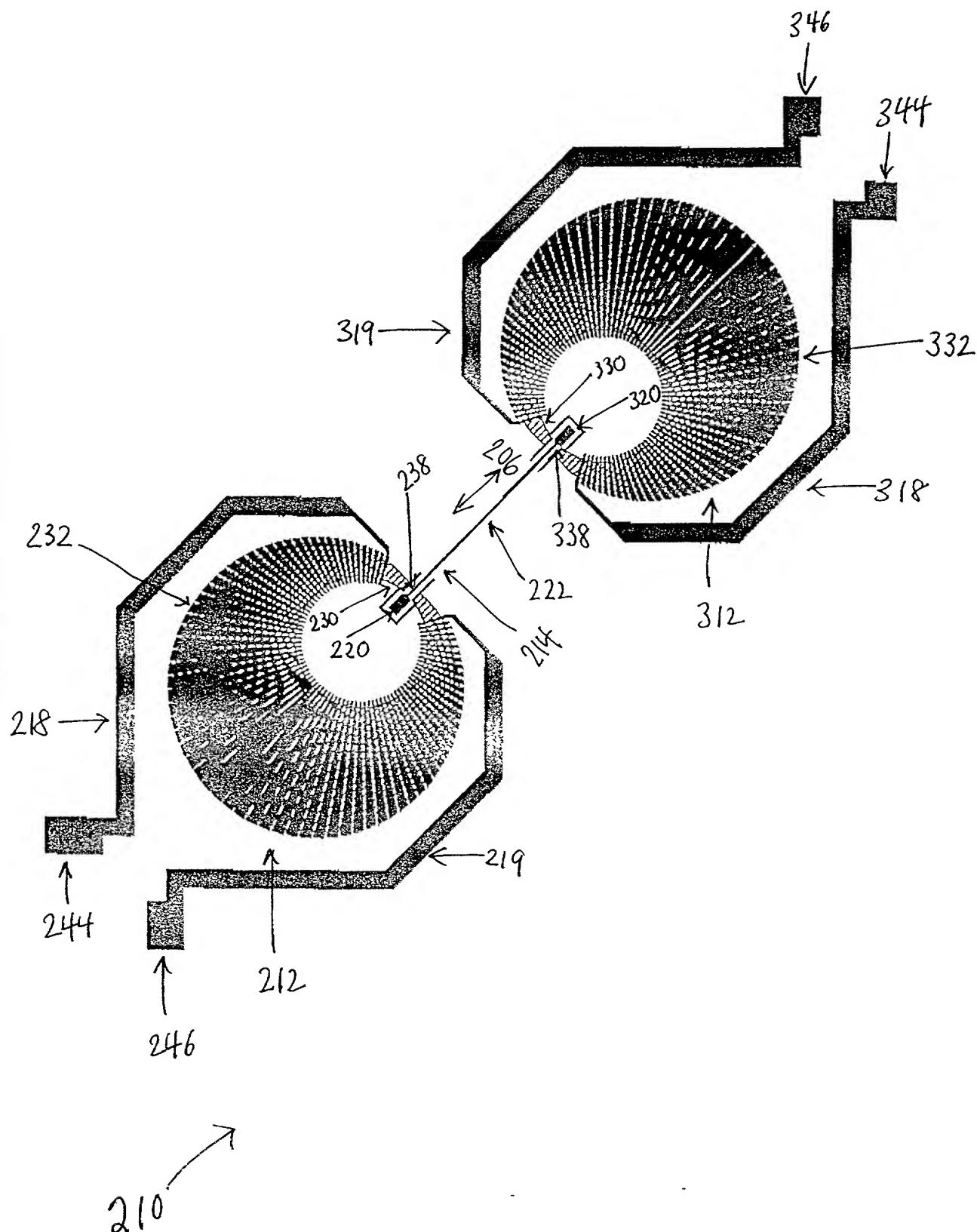


FIG. 11

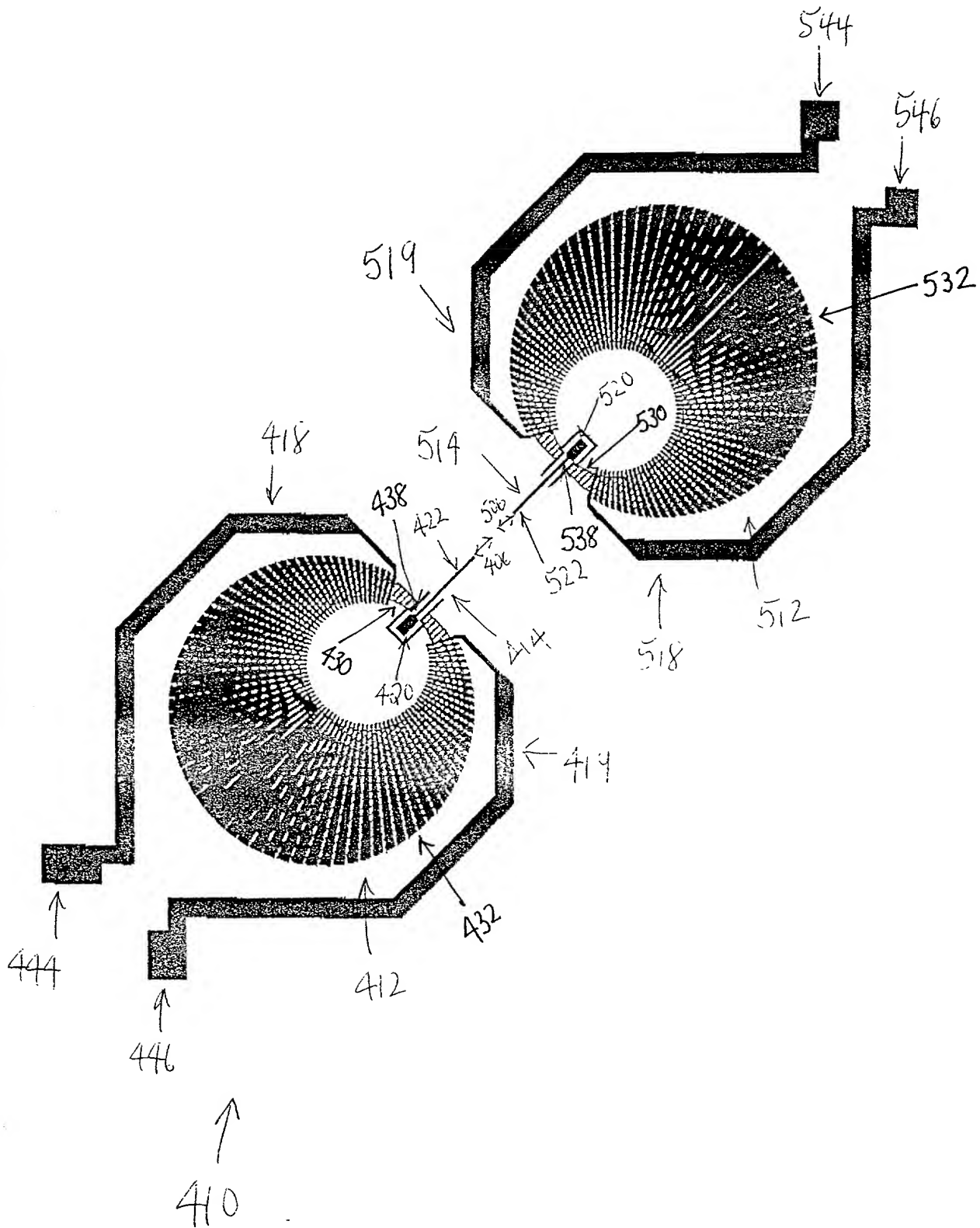


FIG. 12a

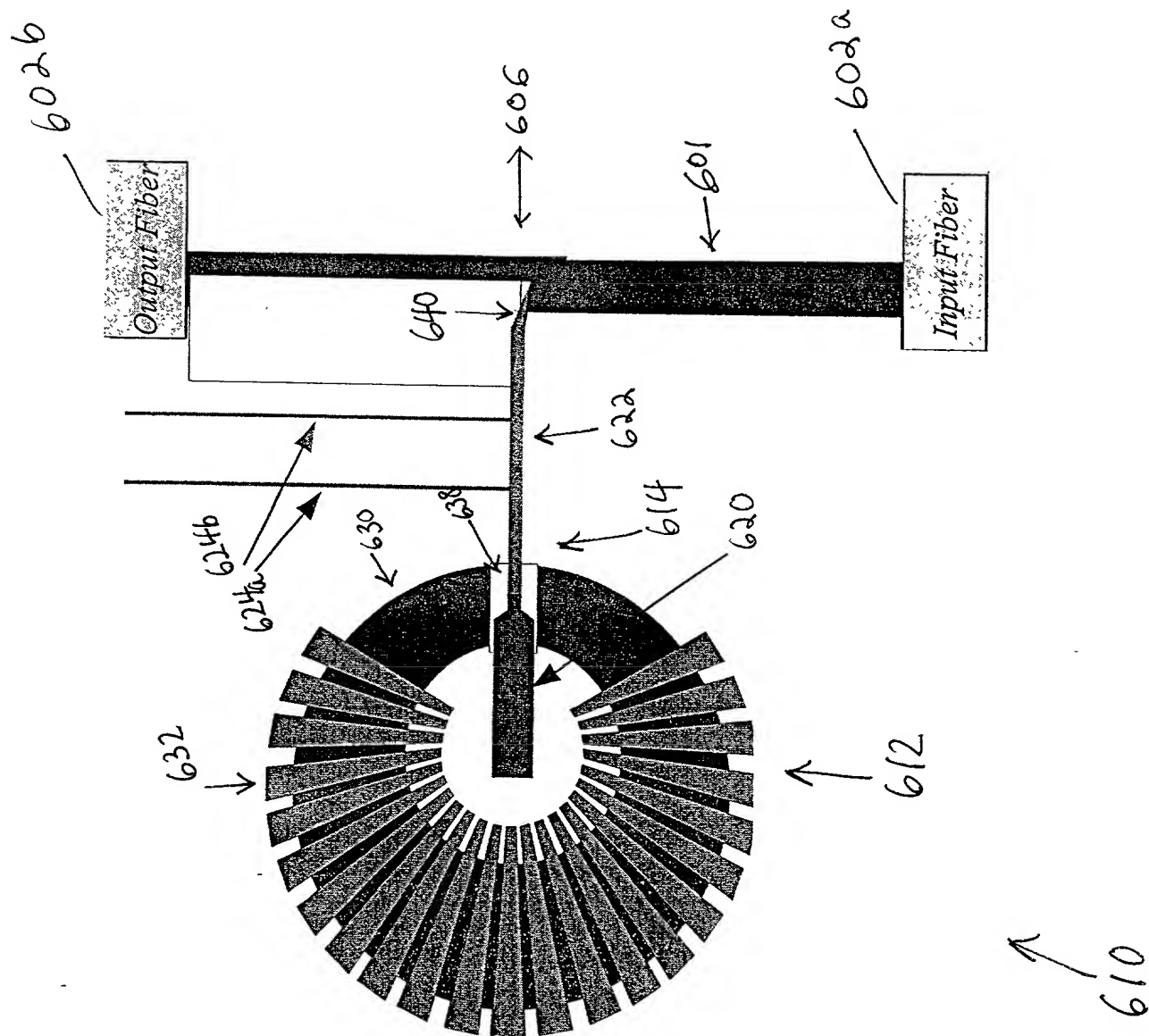
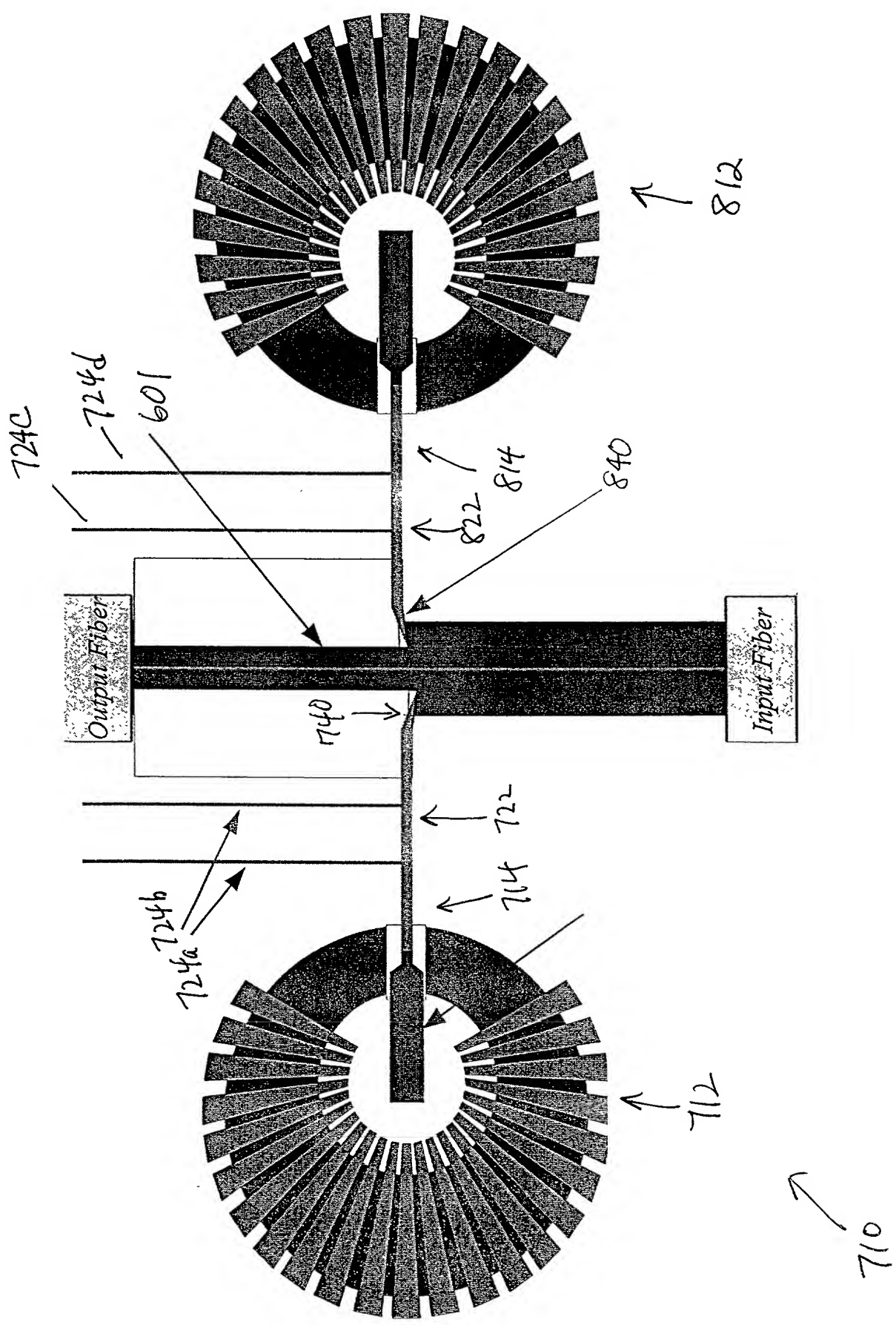


FIG. 13



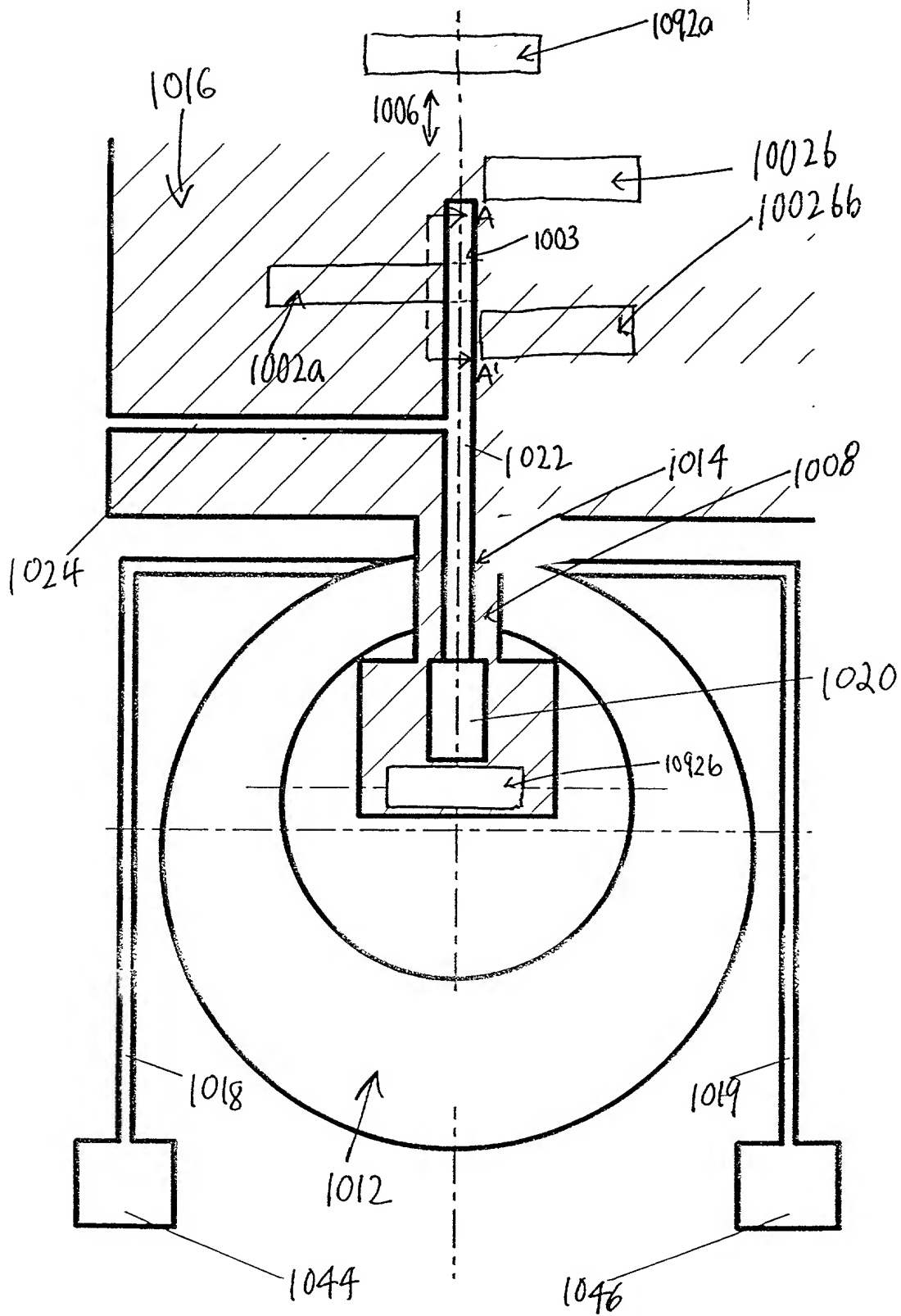


FIG. 15A

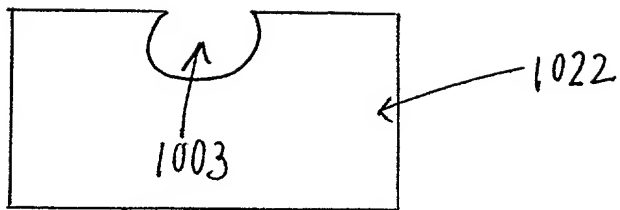


FIG. 15B

10079936.023103

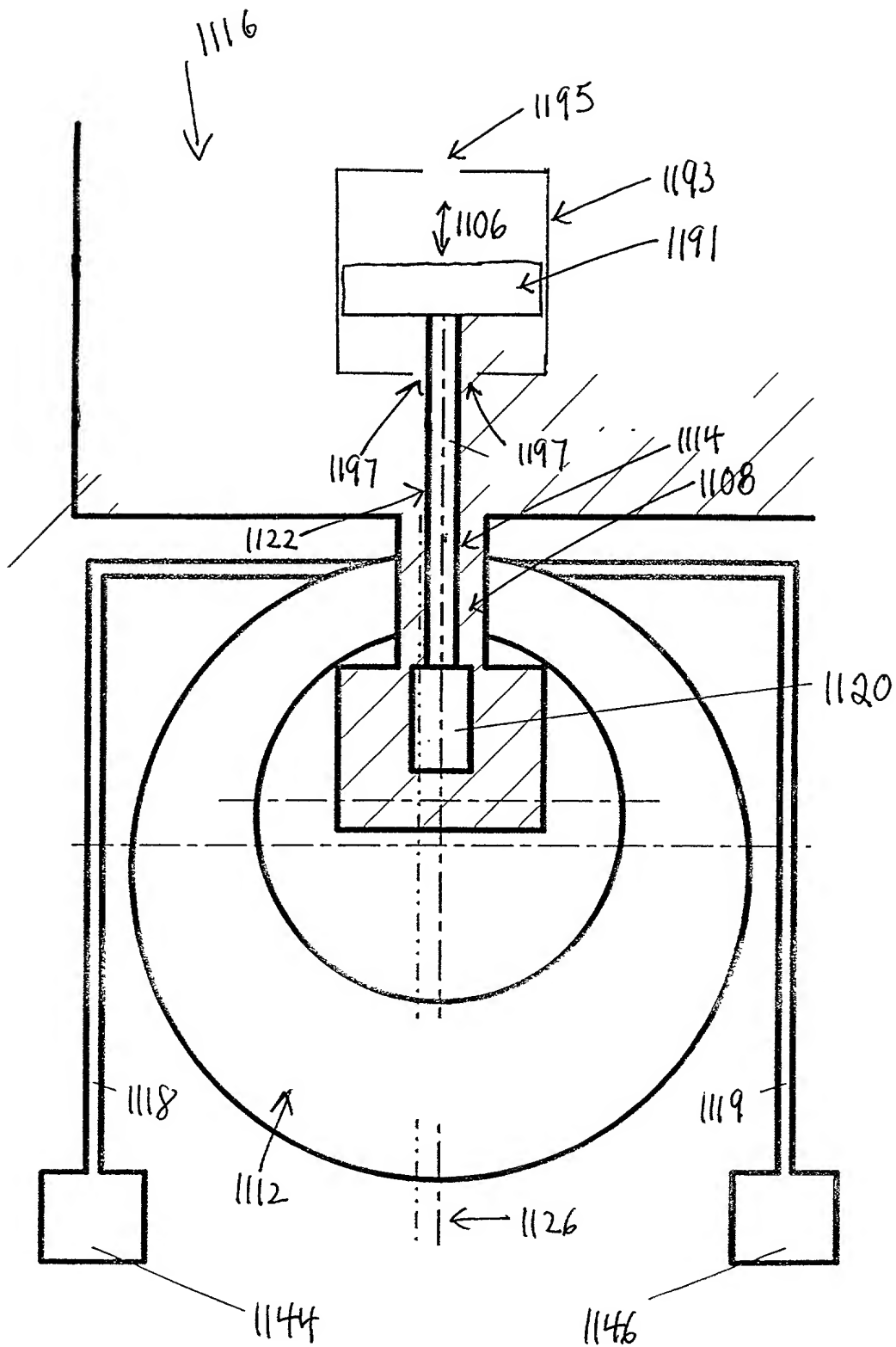


FIG. 16A

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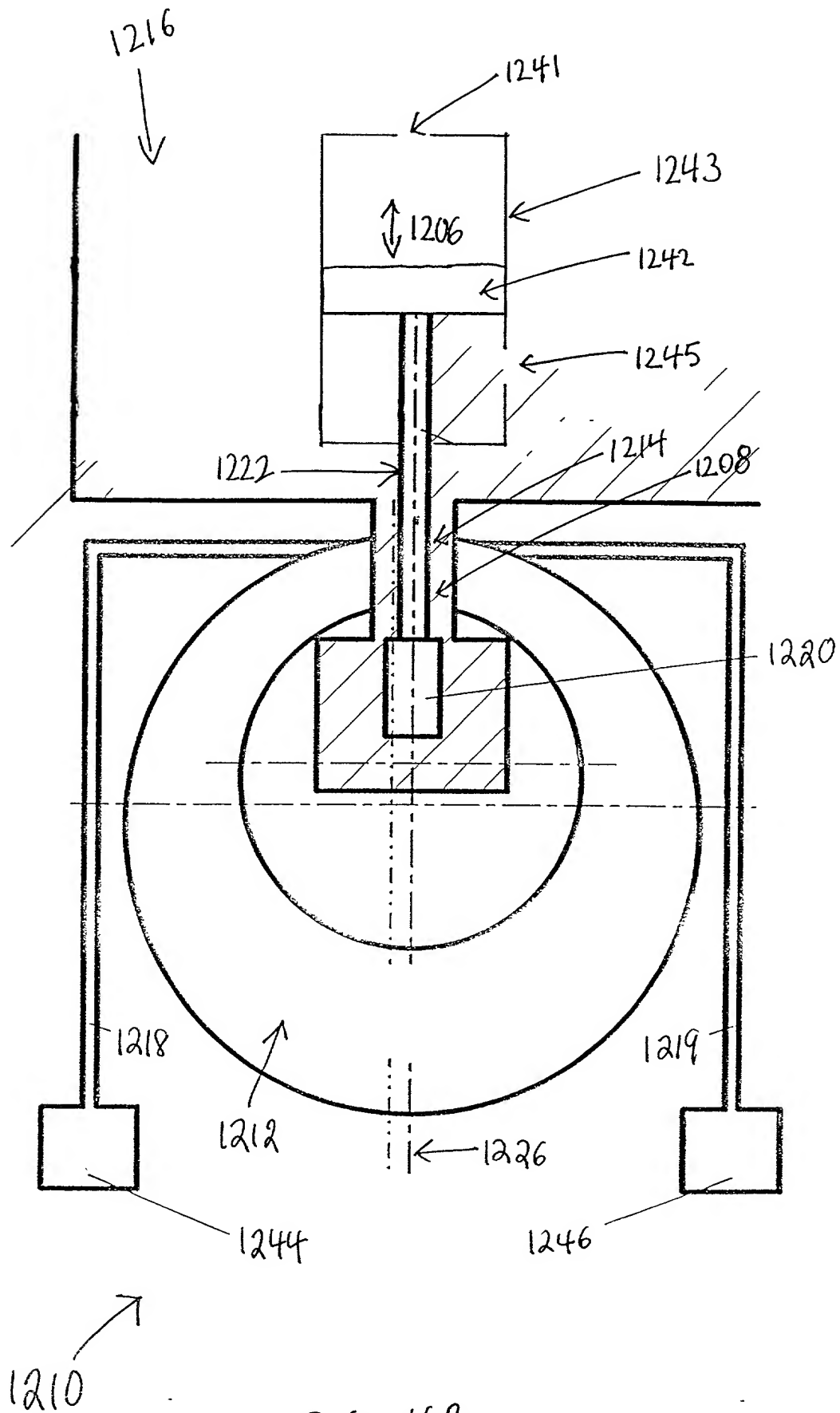


FIG. 16B

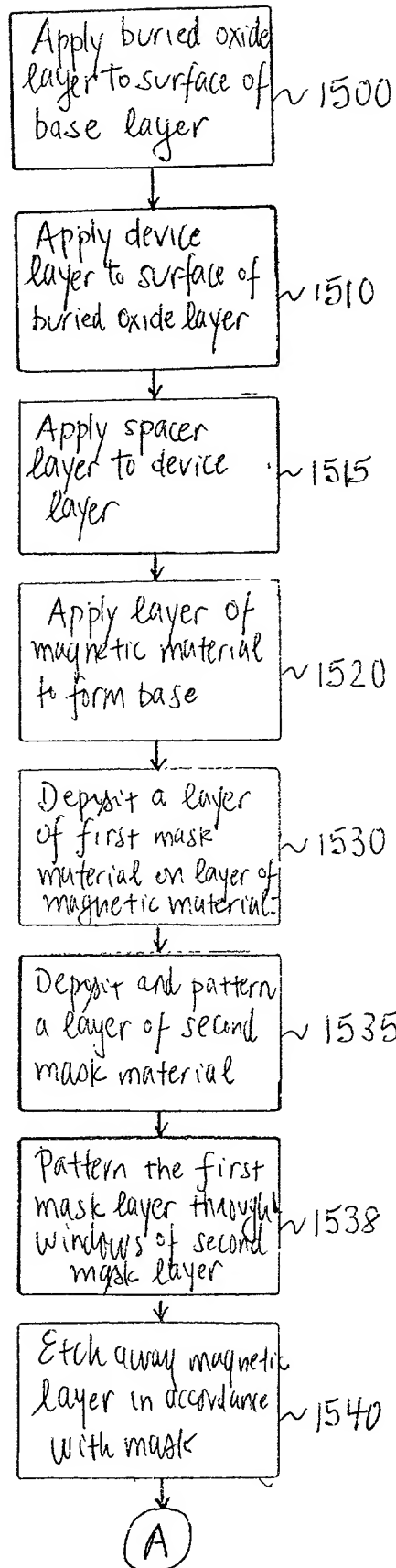


FIG. 17A

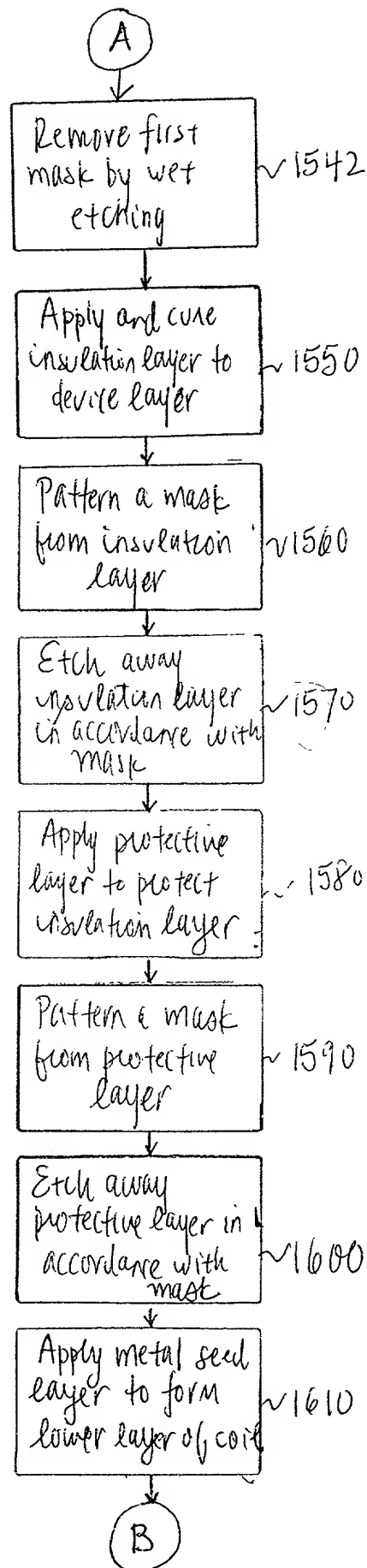


FIG. 17B

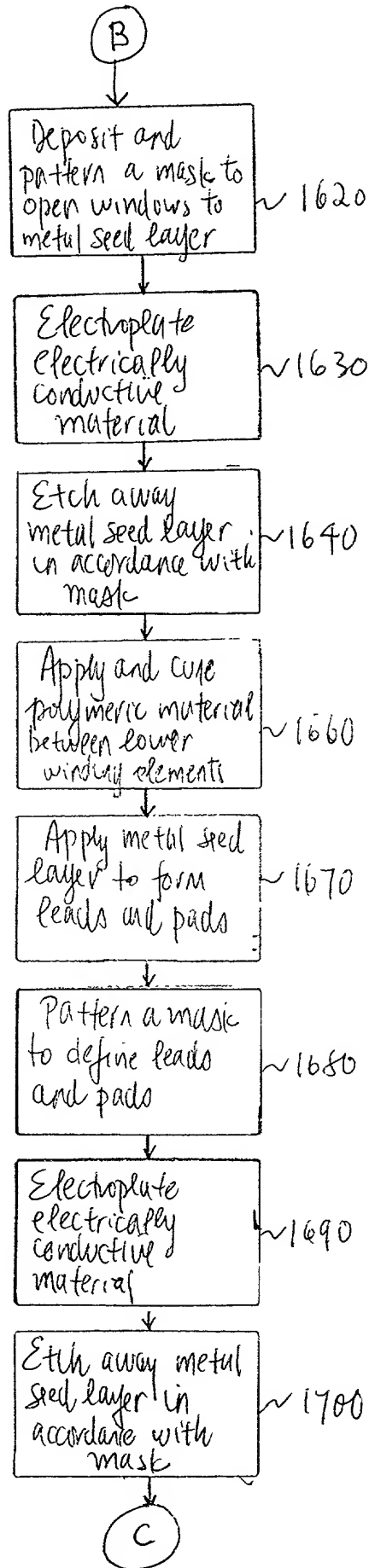


FIG. 17C

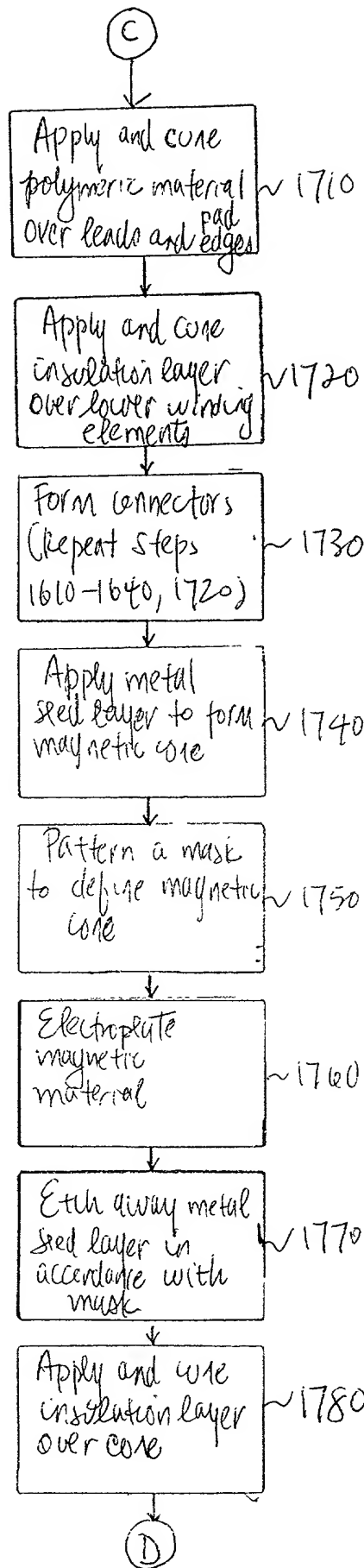


FIG 17D

(D)

Form upper layer
of core and upper
winding elements
(Repeat steps
1610-1660)

~1790

Apply and cure
insulation layer over
upper winding
elements

~1795

Pattern gross
mask

~1800

Repattern gross
mask using mask
of step 1590

~1810

Etch away
protective layer in
conformance with
repatterned mask

~1820

Remove device
layer via deep Si
etching

~1830

Remove buried
oxide layer

~1840

Clean and
dry device

~1850

FIG. 17E